REDVET - Revista electrónica de Veterinaria - ISSN 1695-7504
Vol 25, No. 1 (2024)
http://www.veterinaria.org
Article Received: Revised: Accepted:

Design and Development of Reversible Half adder using an 8*8 reversible logic gate

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Abstract: -
A digital logic circuit that adds two binary single-bit integers is called a half adder. In many different types of processors, adders are commonly used to perform arithmetic and logical operations. In this study, we examine how a half adder works using a recently designed CMOS logic gate. The suggested design and the existing system have been compared using garbage output. The circuits are simulated using the MATLAB program.

Keyword: - Reversible gate, CMOS, garbage output.

Introduction: -
One of the most important components of an irreversible circuit is power dissipation. Landauer's principle states that for each bit of missing data during the computation, the irreversible circuit generates heat dissipation of approximately kTln2 Joules, where T is the absolute temperature and k is the Boltzmann's constant.Moore proposed Moore's law in 1965, according to which integrated chips' total transistor count doubles every 18 months. The number of transistors increased as a result. As a result, the processing capacity of computers has steadily increased because the growing density of transistors leads to higher heat generation from information loss during data computation. C.H. Bennet demonstrated in 1973 that rebuilding circuits with reversible gates will result in minimal power loss in digital circuits. Because of the need for greater processing capacity and less energy usage, researchers are searching for alternatives to classical computing, such as quantum computing. As a result, this is now a key component in the development of reversible computing. Reversible computing in reversible gates does not result in power loss. Reversible logic is used in a wide range of technologies, including quantum computing, optical computing, biotechnology, nanotechnology, and adiabatic CMOS design. A distinct one-to-one mapping between input and output vectors is produced by reversible gates, and vice versa. The reversible gate has an equal number of inputs and outputs. Fan-out and feedback are therefore prohibited. A gate can be made reversible by adding extra wires to its inputs and outputs if needed. Ancilla (constant input) refers to the additional wires added to the inputs, whereas "garbage outputs" refers to the additional wires added to the outputs.

Different designs for reversible half and full adders/subtractors have been proposed by numerous researchers. To get greater performance and less complexity, the designs still need to be improved in terms of the quantity of garbage outputs, quantum cost, and constant inputs. This study presents a new reversible half adder that uses a suggested reversible gate. The improvement of trash output, quantum cost, and constant inputs is the primary feature of the discuss design.

Basic reversible gate:
There are actually numerous reversible gates; some of them are as follows:

1. TOFFOLI GATE -
The Toffoli gate is a worldwide reversible logic gate that was created by Tommaso Toffoli. The gate is 3 by 3. The third bit is inverted if the first two bits are set; else, every bit stays the same. Five is its quantum cost of a. Another name for it is CCNOT, or controlled-controlled not gate.

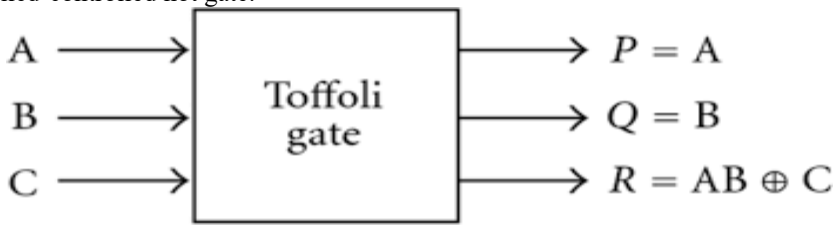

Figure 1: Block diagram of Toffoli gate

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TRUTH TABLE –

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

TABLE1: Truth table of TOFFOLI GATE

2. **Feynmann gate: -**
It has two inputs and two outputs, making it a 2*2 gate. Another name for it is CNOT gate. The quantum cost is one.

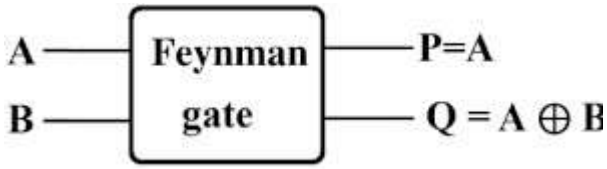

Figure 2: ***Block diagram of FEYNMAN GATE***

TRUTH TABLE –

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

TABLE 2: Truth table of FEYNMANN GATE

3. **Fredkin gate:** -
It's a 3*3 gate as well. It has a quantum cost of five as well. If the first bit is 1, this three-bit gate switches the final two bits. Because we can create many more digital circuits using it, it is a universal gate.

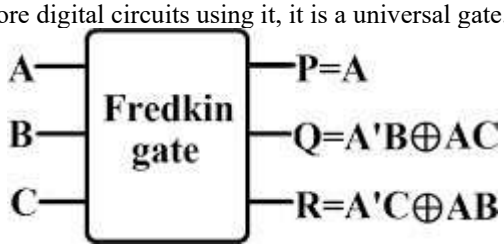

Figure 3: Fredkin gate

A novel reversible gate-
It is an 8*8 reversible gate with 8 inputs and 8 outputs. The gate's quantum cost is 24. This proposed gate name is PRT gate. The proposed PRT-8×8 reversible logic gate is presented along with its input-output structure, Boolean expressions, internal logic organization, block diagram, gate-level circuit, behavior of truth-table and recovery equations. The gate is divided into two four-variable parts and has preserved and computed outputs that are AND and XOR.The 8*8 reversible gate's logic diagram is shown in fig.

8*8 PRT reversible gate-
Its input vector and output vector are presented as follows-
I_v = (A, B, C, D, E, F, G, H), O_V = (P, Q, R, S, T, U, V, W)
Boolean expression is as given below -

$$P=AQ=B\oplus(A\cdot C)R=CS=D\oplus A\oplus C\oplus(A\cdot C)T=EU=F\oplus(E\cdot G)V=GW=H\oplus E\oplus G\oplus(E\cdot G)$$

BLOCK DIAGRAM –
The block diagram of the PRT–8*8 gate has 8 input lines and 8 output lines. The input side A, B, C, D, E, F, G, H and the output side have P, Q, R, S, T, U, V, and W. The block diagram of PRT -8*8 reversible gate is shown in figure.

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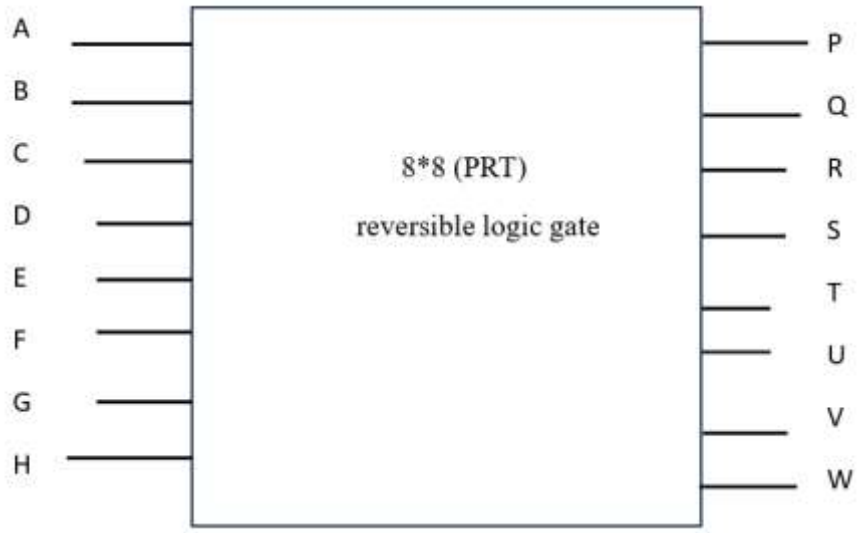

Figure 4: Block diagram of PRT gate

THE GATE-LEVEL CIRCUIT OF 8*8 PRT GATE –

This circuit shows the physical realization of proposed PRT reversible gate equations.

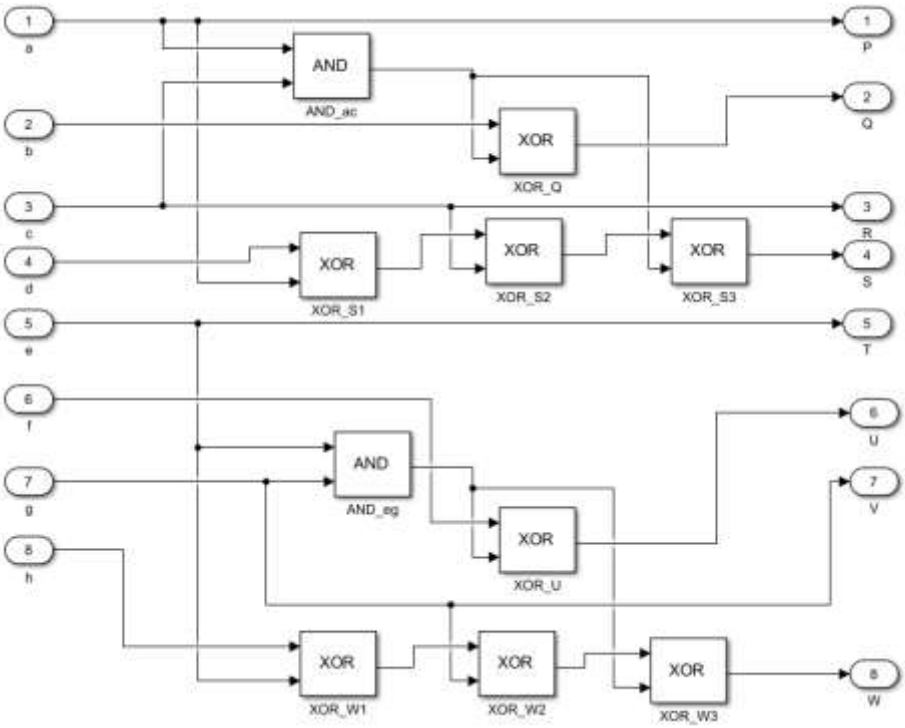

FIGURE 5 Gate-level circuit of proposed PRT reversible gate

TRUTH TABLE— The complete truth table of the proposed PRT reversible gate contains $2^8 = 256$
The selected input and output combinations of the proposed PRT reversible logic gate are shown in table 1.

TABLE 3 Selected truth table of the proposed PRT-8×8 reversible logic gate

Original Row	Category	A	B	C	D	E	F	G	H	P	Q	R	S	T	U	V	W
1	Initial row	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	Initial row	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
121	Middle row	0	1	1	1	1	0	0	0	0	1	1	0	1	0	0	1
246	Final row	1	1	1	1	0	1	0	1	1	0	1	0	0	1	0	1
161	Selected functional row	1	0	1	0	0	0	0	0	1	1	1	1	0	0	0	0

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The Proposed Design –
We used our suggested gate to describe reversible half-adders in this section. The suggested reversible gate is used to create the circuit. In the proposed realization, the proposed PRT reversible gate is used to arise the half adder output by mapping to designated input lines of the proposed PRT reversible gate.

Reversible half adder using new reversible gate –
The PRT reversible gate realizes the half adder function by combining preserved output for the XOR-based sum and the computed product output for the carry. The block diagram of the PRT reversible gate is shown in figure 6.

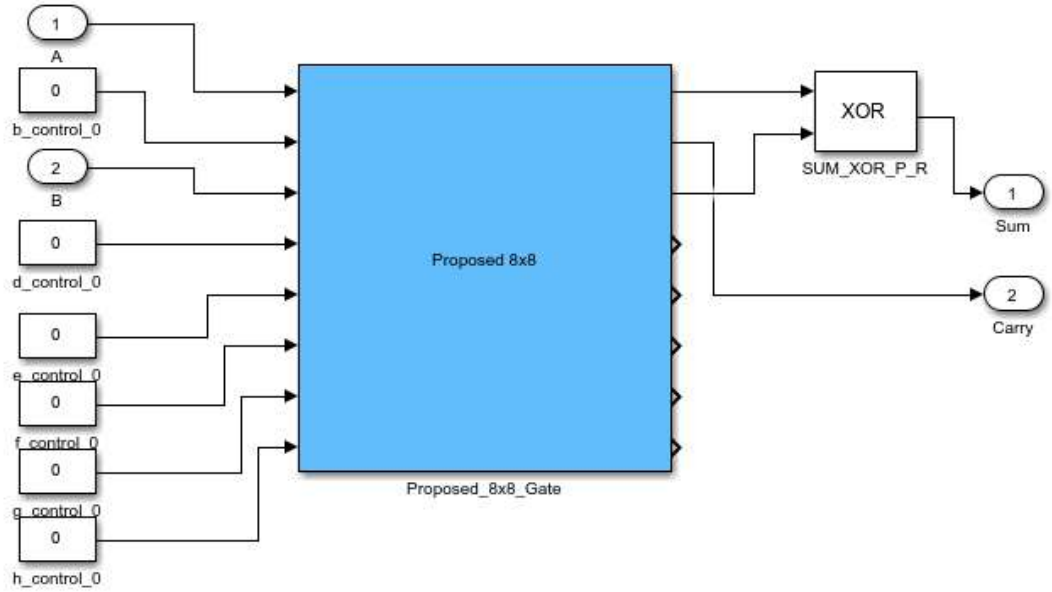

Figure: 6

TRUTH TABLE –
The truth table of a half adder using a PRT reversible gate is given below.
Truth table of half adder using PRT-8×8 gate

A	B	Sum=P⊕R	Carry=Q
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Result and Discussion –
It is possible to provide the suggested design as the most effective one for reversible circuits. The MATLAB simulator tool is used to simulate this design. The simulated waveform is displayed in the figure below. The concept of reversible logic enhances the effectiveness and functionality of digital systems.

In this research, we presented a method for designing a half adder circuit using a newly proposed reversible gate. In this, we designed half adder circuits using the suggested gate.
The given table confirms that the anticipated PRT-reversible logic gate-based half adder produces correct sum and carry values for all binary input combinations. The actual outputs match the expected outputs in every case.
Half-adder result using PRT-8×8 gate

A	B	**Expected Sum**	**Expected Carry**	**Actual Sum**	**Actual Carry**	**Verification status**
0	0	0	0	0	0	Passed
0	1	1	0	1	0	Passed
1	0	1	0	1	0	Passed
1	1	0	1	0	1	Passed

The signal results of the suggested half adder using the anticipated PRT reversible gate is shown in figure 7. The waveform chains the tabular result.

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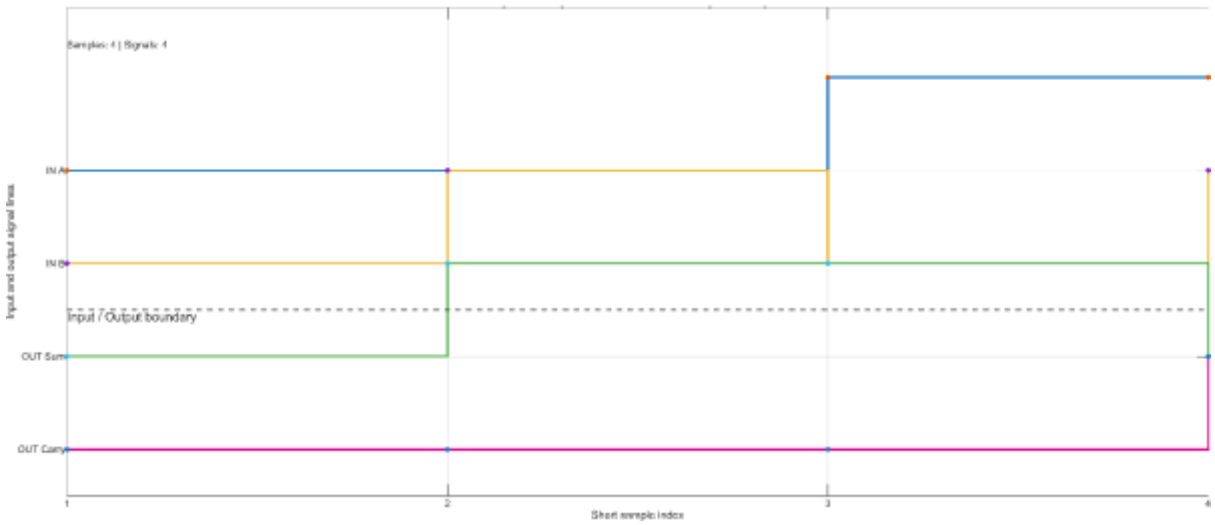

FIGURE 7: Waveform of half adder using PRT reversible gate

The result of the half adder indicates that the proposed PRT reversible logic gate is able to perform the arithmetic operation correctly. The proposed gate can be used in other applications that are reversible subtractors, multiplexers, encoders, decoders, shift registers and more complex ALU circuits.

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