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Addressing the Bottlenecks in IoT and 5G Integration: A Study on Existing **Implementation Issues and Challenges**

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Abstract:

The integration of Internet of Things (IoT) and Fifth-Generation (5G) networks is a transformative development that promises enhanced connectivity, reduced latency, and increased device density, fostering innovations across various industries. The seamless integration of IoT devices with 5G networks faces several significant challenges and bottlenecks, which hinder the realization of its full potential. This paper presents a comprehensive study on the existing implementation issues and challenges associated with the convergence of IoT and 5G. Key areas of concern include network architecture limitations, security vulnerabilities, interoperability between devices and protocols, spectrum management, and the scalability of infrastructure to handle massive IoT deployments. Furthermore, issues related to energy consumption, latency, and quality of service (QoS) requirements are explored in the context of real-time IoT applications. Detailed analysis of current research and case studies identifies the critical bottlenecks and proposes potential solutions for overcoming these hurdles. The findings provide valuable insights for researchers, network providers, and industry professionals working towards optimizing the integration of IoT and 5G technologies for future applications.

KEYWORD: IoT and 5G Integration, Network Challenges, Connectivity Issues

1. Introduction

The convergence of the Internet of Things (IoT) and fifth-generation (5G) wireless technology is poised to revolutionize industries by enabling ultra-reliable, low-latency communication and supporting a massive number of connected devices. This integration is critical for realizing futuristic applications such as smart cities, autonomous vehicles, remote healthcare, and industrial automation. While 5G offers unprecedented advantages in speed, bandwidth, and network slicing capabilities, the practical integration with IoT ecosystems remains a complex and evolving challenge.

Despite the theoretical potential, the implementation of IoT-5G integration faces numerous bottlenecks. These include interoperability issues between heterogeneous devices, scalability constraints, energy efficiency concerns, spectrum allocation complexities, data security vulnerabilities, and challenges in maintaining consistent Quality of Service (QoS). Moreover, the fragmented regulatory landscape and lack of standardized protocols further exacerbate these difficulties, particularly in developing economies.

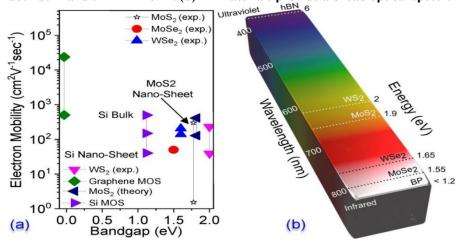
At the moment, silicon technology has several difficulties due to its small device dimensions, particularly its shorter channel lengths. To lessen the impacts at lower channel lengths, new technologies like as SOI, FinFETs, etc., have been developed and effectively deployed. Beyond certain channel lengths, these systems are still seen to be saturated in terms of scalability. On the other hand, other concepts that may use various materials have been advanced beyond existing CMOS technologies. One of the methods is 2D material-based technology, which was created by exfoliating graphitecrystal to create a 0.4 nm thick graphene layer. Numerous studies on comparable materials that produce such thin layers have been prompted by this innovation and its methodology. Graphene has undergone extensive study to be used into commercial technologies because to its very high mobility and several other intriguing qualities.

However, its applicability to logic circuits were limited by the absence of bandgap. Transition metal dichalcogenides (TMDs) are a type of semiconducting layered materials that have demonstrated promise for such applications due to their suitable band gaps. In addition to these novel materials, such as transition metal mono-chalcogenides, the dichalcogenides (TMDs) are a type of semiconducting layered materials that have demonstrated promise for such applications due to their suitable band gaps. In addition to these novel materials, such as transition metal monochalcogenides, the layered structure of tertiary compound semiconductors and topological insulators has also been studied.

Article Received: Revised: Accepted:



Figure 1: (a) Comparison of the band gap and charge carrier mobility provided by several 2D materials with Si in both bulk and thin film form. (b) 2D materials provide a broad optical spectrum.



A wide range of applications, including gas sensing, quantum computing, RF devices, logic, memory, and energy-saving applications, are anticipated for these materials due to their remarkable qualities [1]. These materials are anticipated for heterogeneous integration of electronics, optoelectronics, and quantum computing systems with these applications. In light of the changes, a roadmap has also been suggested. Despite their outstanding qualities and numerous potential uses, these materials face considerable difficulties in experimental implementation. These include the issues of technology, process development, and dependability, which are covered in more detail in the sections that follow. Generally speaking, the channel material must be shaped into the appropriate nano scale form or dimension for all feasible device applications utilizing a semiconducting channel. The channel material is often etched using a hard mask, either wet or plasma or lithographic mask to mask the appropriate active region. Atomically thin layered materials have proven challenging to etch with plasma. The atomically thin surface is either attracted to the resist or the ultra-thin and delicate layered substance gets damaged by the plasma. Wet etching can't provide ultra-sharp edges and results in isotropic etching, which might lead to edge states [2]. Despite the paucity of research on defect-free methods, there have been some early attempts to etch the material in order to reduce its thickness for MoS2. Wet chemistry based on HNO3 is used in the initial attempts. Using this technique, the material is etched down to a monolayer layer by layer. The material is initially oxidized by the HNO3 reaction with MoS2, and the oxidized portion is then dissolved in the solution. Thin material is left behind when oxidation is difficult at lower thicknesses. Dry oxidation, however, uses the same oxidation technique.

It is important to note, nevertheless, that none of these methods were investigated while the resist material was present over the active region. Oxygen plasma has been a commonly utilized method for patterning monolayer TMDs, especially CVD MoS2. However, it is incredibly time-consuming to employ oxygen plasma for patterning few-layer TMDs. Furthermore, there is little information on how oxygen plasma affects channel characteristics after patterning or etching [3]. While eliminating the resist layer, a lengthy etching period may also harden the resist and ultimately harm the ultra-sensitive surface. Additionally, enough resist residue is left in the active region by solidified resist, which severely degrades the channel's characteristics. Additionally, it is not recommended to expose resists to oxygen plasma for an extended period of time because this can complicate the process by etching commonly used resist materials.

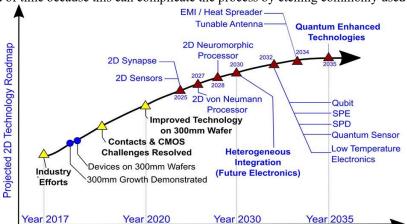


Figure 2: Projected roadmap for 2D materials towards a range of uses

Vol 25, No. 2 (2024)

http://www.veterinaria.org

Article Received: Revised: Accepted:



The development of 2D materials, compatible dielectrics for these materials, large-scale integration, etc., are further process hurdles. It is usually difficult to develop these materials on a target substrate in a high-quality manner [4]. As an alternative, it is shown that these materials can develop on metallic substrates and then be transferred onto other substrates of choice. However, the procedure presented difficulties such as the production of wrinkles, defects, and accidental doping from the transfer process. Finding dielectrics that work with these materials is the next challenge. Due to the lack of dangling bonds, dielectric development is extremely unlikely on these materials. As an alternative, the transfer of grown dielectrics has been shown to present comparable difficulties.

One such issue that needs to be carefully addressed for the dependable operation of MoS2-based circuits is drain current hysteresis and threshold voltage instability in MoS2 FETs. Because of their high surface-to-volume ratio, this problem generally affects all TMDs. Although these studies offered a range of experimental findings, the original studies lacked physical explanations for why the observed instabilities should result from the adsorption of moisture or oxygen. Still, it was said that adsorption of a particular molecule would cause charge transfer because of the huge surface-to-volume ratio, which would cause the hysteresis observed in the I-V characteristics [5]. Nevertheless, in further research, the same has to be measured and confirmed using atomistic computations or direct methods. For instance, by extending findings from (i) research on the adsorption of water molecules on MoS2, which increases the lubricating efficacy of MoS2, and (ii) hysteresis seen in ZnO nanowire in the presence of O2, the authors suggested charge transfer from/to absorbed molecules as the primary cause.

2. Review of Related Literature

Zhang et al. (2019) explored the primary technical challenges in integrating IoT and 5G. They identified network congestion, latency issues, and energy consumption as major obstacles. Their study emphasizes the need for intelligent network management to handle the massive volume of devices that 5G is expected to support.

Chen et al. (2020) analyzed the bottlenecks in resource allocation when integrating IoT with 5G networks [6]. Their research focuses on optimizing spectrum management and ensuring that the diverse IoT devices can efficiently access network resources without degrading the quality of service (QoS) for other users.

Zhou and Wang (2021) reviewed security issues in the convergence of IoT and 5G networks. The study emphasizes vulnerabilities in data transmission, device authentication, and overall system integrity. Given the increasing number of connected devices, ensuring robust security protocols is identified as a significant bottleneck.

Hassan et al. (2022) focused on the scalability challenges in IoT and 5G integration. They pointed out that as IoT devices continue to proliferate, scaling the infrastructure to support these devices is a growing issue. They also highlighted challenges in managing the distributed networks that span across different sectors and applications.

Li et al. (2023) conducted a study on the role of network slicing in the IoT-5G ecosystem. Network slicing is a potential solution to optimize IoT and 5G integration, but they identified that poor implementation of network slices could lead to bottlenecks in service delivery, especially in time-sensitive applications such as autonomous vehicles or smart healthcare [7].

Wang et al. (2024) identified the lack of standardization in IoT and 5G integration as a significant challenge. They discuss how different protocols and technologies used by IoT devices create barriers to seamless communication with 5G networks. The study advocates for unified standards and protocols to enable better interoperability.

Singh and Soni (2025) examined how edge computing can alleviate some of the latency and processing bottlenecks in IoT-5G integration. They found that offloading computational tasks to the edge of the network could reduce latency and enhance performance, but it introduces challenges in terms of resource allocation and data synchronization.

To acquire required dimensions, this study studies the patterning of two-layer Significant resist residue from the SF6 plasma left on the mask TMD layers, allowing for faster TMD etching. This was clarified by F-radicals' greater diffusivity over the resist-TMD interface, as well as the substantial reactivity of SF6 plasma. Significant channel degradation resulted from this, as seen by a notable decrease in ON current and a notable rise in OFF current. At a well controlled rate CHF# plasma showed lower etch rate. Raman spectroscopy suggests that the F-doping also produced a compressive strain across the material; we confirmed this using field-effect mobility extraction. We discovered that doping reduced contact resistance and field-effect mobility.

It was demonstrated that there was a clear correlation between the degree of doping, proximity resistance, and field-effect mobility; the higher the level of doping, the lower the resistant to contact.

Unintentional doping caused mobility loss, but it also dominated the transistor's properties, resulting in a decrease in ON current and a rise in OFF-state current.

3. Research Methodology

The band structure and density of states of pure MoS2 crystals without oxygen or water molecule adsorption are compared to the same. There is no discernible change (\approx 2.5meV) in the Fermi energy level (EF) caused by water adsorption. In contrast, the addition of two additional levels inside the MoS2 energy band gap has resulted in a notable downward shift of \approx 0.36eV in EF in oxygen absorption [9]. As a result, MoS2 becomes substantially doped when oxygen is added. Furthermore, it can be observed that the two newly generated levels, which are separated by only a few meV, are slightly above and below EF in the later scenario. Here, however, we measure and verify that the shift in the work function is due only to the presence of oxygen and is not affected by the concentration of moisture. It is therefore

Vol 25, No. 2 (2024)

http://www.veterinaria.org

Article Received: Revised: Accepted:



worthwhile to investigate whether the introduction of oxygen or moisture merely affects the Fermi level or if it also leads to a countable number of mid-gap states.

The above-mentioned DFT simulations of the adsorption of water molecules, which demonstrate a little impact on the band structure, are in contrast to the experimental results reported by Late et al. More research is need on this. The third possibility is the existence of S defects or vacancies, which frequently causes MoS2 FETs to behave in the n-type. In light of this, we have examined the density of states and band structure of the MoS2 crystal in the presence of oxygen or water molecules, taking into account the S defect.

Three different states are produced by moisture adsorption over the S defect: shallow donor, deep donor, and deep acceptor trap. Additionally, the Fermi energy level is moved 70meV above the mid-gap location, making it intrinsic to nature, when previously it was n-type in the presence of merely S-defect. Likewise, the impact of O2 adsorption on S. Similar to O2 adsorption over pristine crystal, it has been shown that the oxygen atom over S defect produces a deep acceptor state and a donor state with degeneracy with a conduction band. In this instance, the material remained n-type because the Fermi energy level was mostly constant at 0.22 eV (it was 0.254 eV with the S defect) [10].

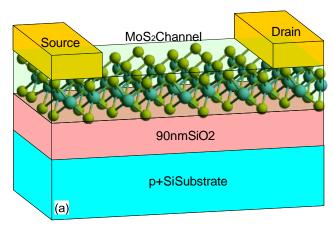


Figure 3: Mos2Fets Accomplished

The maximum DoS of the valence and conduction bands of pure MoS2 is comparable to or greater than the peak density of states caused by the S defect. In comparison to the other states found inside the bands, this makes it at least 25×degenerate. The change in EF by ≈0.25eV above the mid-gap position is quantified by this degree of degeneracy. Due to identical DoS of induced acceptor and donor levels, H2O is adsorbed over the S defect. This causes donor and acceptor traps to compensate for their existence, shifting EF to the mid-gap position. A deep acceptor level with noticeably strong DoS is evident when O2 is adsorbed over the S defect. The trap state caused by O2 adsorption over the intrinsic MoS2 crystal is known as TL3. Because it is below the mid-gap and a degeneracy of about 100, it is a strong acceptor level. The sulfur flaw in the MoS2 crystal causes the TL6 is the trap state. Its location close to or above makes it a deep donor, requiring a comparatively large activation energy to ionize. When there is absorption of water (i.e., water molecules covering the sulfur defect), the trap states brought on by sulfur flaws) are TL8 and TL9. TL2 is the trap state that results from O2 deposition over the sulfur defect in MoS2.

It is in a deeply accepted state due to its proximity to the valence band. The trap states that result from a sulfur defect with O2 adsorption in its vicinity are TL4, TL5, and TL7. While TL4 and TL5 operate as acceptor levels when they are present below mid-gap, TL7's existence makes it a donor level.

Table 1: An overview of the variables that affect hysteresis and the corresponding trap levels

| Influencing factor | DominantTrapLevels | Source of Trap Levels | | |
|-----------------------|--------------------|------------------------------|--|--|
| Atmosphere | TL9,TL8andTL7 | Moisture | | |
| Temperature Gate Bias | TL5,TL4andTL3 | Moisture and Sulfurd effects | | |
| _ | TL9,TL8andTL7 | Moisture and Sulfurd effects | | |

In actuality, when the sample is subjected to atmospheric conditions (ATP), all of the aforementioned trap states should be present. On the other hand, trap states caused only by sulfur defects or vacancies are anticipated to exist at low pressure and vacuum (LP) circumstances. Trap states caused by water adsorption are anticipated to be absent at high temperatures. When compared to the device tested at atmospheric pressure conditions, the device measured at low pressure exhibits reduced hysteresis. Gate voltage IDrain–Dis is compared with the corresponding drain current shift between forward and reverse sweeps. The device's IDrain–D is 3× bigger at atmospheric pressure than it is in vacuum, suggesting that atmospheric circumstances have a significant impact on the device's properties. Anti-clockwise hysteresis is confirmed by positive IDrain–D, which is consistent with previous findings. Here, the existence of one or

Article Received: Revised: Accepted:



more donor states (TL6, TL7, TL8, and TL9)—which are probably present in atmospheric circumstances, as described in the preceding section is responsible for the positive shift that results in anti-clockwise hysteresis. The presence of only one deep donor state, TL6, which is ascribed to the sulfur defect in the MoS2 crystal, results in a lower drain current shift under LP conditions. However, the presence of additional low donor states (TL7, TL8, and TL9), especially TL9, which has the least ionization energy, is also responsible for the larger drain current shift under ATP conditions. All of these donor states are anticipated to exist in the presence of moisture over sulfur defects or sulfur defects alone, as previously discussed [12].

4. Result Analysis

FETs and TLM test structures of circuit lengths as low as 300 nm were formed using e-beam lithography with PMMA as the resist material. For source/drain, Ni/Au (20/50 nm) was placed preferentially connections using e-beam evaporation, followed by metal lift-off and thermal annealing. Additionally, KI salt is mixed with DI water to create a 2% concentration KI solution. When different KI concentrations were first tested, it was discovered that 2% produced the greatest increase in device performance. The device's performance didn't get any better when the KI concentration was raised over 2%. The MoS2 sample was fully submerged in the solution for five minutes at room temperature following the full dissolution of the KI salt [13]. We prepared massive samples using and with no KI treatment for extremely high-resolution XPS examination. In order to experimentally establish the effect of KI doping. These samples had a dense dispersion of flakes because they were mechanically exfoliated over cleansed SiO2/Siwafer with a significant proportion of MoS2 crystal. Sulfur has two peaks, and molybdenum has three. a clear blue shift, between 228.9 and 229 eV.

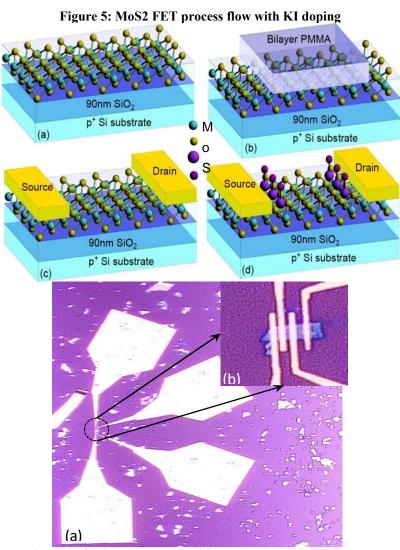


Figure 5: Optical image of MoS2FET and TLM test structure

Vol 25, No. 2 (2024)

http://www.veterinaria.org

Article Received: Revised: Accepted:



Because contact and channel resistance are decreased using KI-based surface charge transmit doping, the ON current of the KI-doped device was shown to increase by $2\times$. It should be mentioned that KI-doped devices' OFF-state current was less than $10\text{pA}/\mu\text{m}$ and remained undamaged. It has been demonstrated that contact resistance has a significant impact on field-effect mobility; lowering this resistance increases field-effect mobility. Additionally, we ascribe the improved field-effect mobility and ON current to the reduced contact resistance. In contrast to the traditional ion implantation-based doping, the enhanced mobility further indicates that the suggested doping does not result in doping-dependent mobility deterioration.

Practically speaking, introduced doping must be stable in the face of environmental changes. Previous research has demonstrated that the ambient atmosphere affects the stability of dopant. While a little decrease in ON current can be ascribed to repetitive stressing of the device, a marginal change in threshold voltage demonstrates doping stability. It may be inferred that there was little to no deterioration in the channel's characteristics because the peak channel mobility did not change after two months [15]. These findings support the suggested doping scheme's resilience in the face of environmental changes.

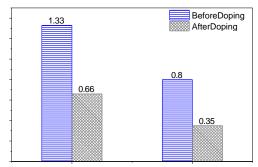


Figure 6: Contact resistance for (a) WSe2 and (b) MoSe2 FETs is compared before and after doping.

Dashed lines show the equal-performance contour and illustrate the nearly square law rise. It is evident from these features that KI doping out exceeds the majority of the previously published approaches, analyzes the KI doped MoS2 FET's figure of merit parameters in this study and contrasts them with those found in prior contact engineering publications. Using KI solution, we present a "stable charge transfer doping" method for MoS2 thin flakes. It was discovered that KI doping, which causes KI molecules to adsorb across the MoS2 surface at the M site, non-degenerately dopes the MoS2 layer close to the S/D metal and channel edge. ON current up to $500\mu A/\mu m$ and field effect mobilities over 70cm2/Vs were obtained while retaining an ON to OFF ratio well above 106 using KI doping contact resistance as low as $0.75k\Omega - \mu m$.

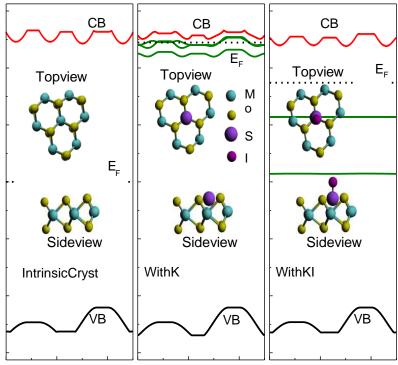


Figure 7: Mos2 Crystal Pristine

Vol 25, No. 2 (2024)

http://www.veterinaria.org

Article Received: Revised: Accepted:



Electron beam evaporation is used to install the metal stack of Ni/Au (10nm/60nm), which is then pulled off to obtain back-gated TLM structures with various channel lengths (300nm, 500nm, 800nm, and 1000nm). TLM test structures were employed for contact resistance extraction. We evaluate the material/channel quality following exfoliation and post-device manufacturing in terms of physical flaws, uniformity in channel.

An absence of doping or charge transfer in the channel area as a result of KI adsorption is shown by the lack of threshold voltage change in the presence of increasing OFF-state current. It should be mentioned that MoSe2 FETs exhibit a greater rise in OFF-state current than WSe2 FETs. This indicates that the channel material also affects the introduction of R-G centers or the energy level of induced mid-gap states caused by KI. The next part presents further insights into the events causing the doping utilizing band structure calculations based on density functional theory while taking metal atoms and KI into consideration across WSe2 and MoSe2.

Table 2: Performance indicators attained in this study are compared to those in previous studies. S.T. stands for sulfur treatment, G.E. for graphene electrodes, and P.E1 for phase engineering in the contact region.

| Reference | ION (μA/μm) | RC (kΩμm) | μ FE (cm2 /V s) | Maxgm (μS/μm) | ION IOFF |
|-----------|-------------|-----------|---------------------|---------------|----------|
| P.E1 | 87 | 0.2 | 46 | 86 | 107 |
| P.E2 | 1260 | - | 27 | - | 106 |
| G.E | 870 | 0.54 | 108 | - | 104 |
| C.D | 430 | 0.5 | 78 | - | 106 |
| Ni.G.E | 470 | 0.2 | 95 | - | 105 |
| S.T | 180 | 5.64 | 28.6 | - | 107 |
| KI Doping | 500 | 0.86 | 74 | 13.98 | 106 |

Table shows how doping improves the mobility of FETs, showing that enhanced carrier injection at contact edges—rather than universal doping injected across the channel—is responsible for the increase in ON-state current. Figure which contrasts extracted contact resistances prior to and during doping, validates a decline in the contact resistance. MoSe2FET has a 2.3× decrease in contact resistance, whereas WSe2FET displays a 2.0× decrease.

5. Conclusion

The integration of the Internet of Things (IoT) with 5G technology presents immense opportunities for enhancing connectivity, enabling real-time communication, and supporting the exponential growth of connected devices. However, this integration is accompanied by several significant bottlenecks that need to be addressed to ensure its seamless implementation and optimal performance. The primary challenges identified in this study include network congestion, resource allocation inefficiencies, security vulnerabilities, latency issues, and the lack of standardization. Network congestion and latency, in particular, hinder the real-time capabilities that 5G promises, especially in critical applications like autonomous vehicles, smart cities, and healthcare systems. Furthermore, the rapid increase in the number of IoT devices demands efficient resource management to avoid network overloads and ensure Quality of Service (QoS) for all users. Security and privacy concerns remain significant, given the massive volume of data exchanged between IoT devices and 5G networks. The vulnerabilities in device authentication and the potential for cyberattacks make robust security protocols a priority. Additionally, the scalability of the network and the ability to manage large-scale, distributed IoT systems remain critical hurdles that need solutions for seamless integration. To overcome these challenges, several solutions have been proposed, including network slicing, edge computing, and enhanced standardization of protocols across IoT and 5G systems. Network slicing offers the potential to tailor network resources for specific use cases, improving performance and reducing congestion. Edge computing helps reduce latency by offloading processing closer to the end devices, enhancing responsiveness. Standardization across IoT devices and communication protocols is essential to ensure interoperability and smooth integration across diverse systems.In conclusion, while IoT and 5G integration is still in its early stages, addressing the identified bottlenecks through innovative solutions like network slicing, edge computing, and enhanced security frameworks is crucial for realizing the full potential of this convergence. Continuous research, collaboration among stakeholders, and the development of new technologies will be key to overcoming these challenges and enabling a truly connected future.

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